

# Linearity Enhancement of Folded Cascode LNA for Narrow Band Receiver

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**ABSTRACT:** In this paper linearity enhancement technique for folded cascode LNA (Low Noise Amplifier) at low voltage operation are presented. To achieve high linearity this FC-LNA adopted MDS technique at CS (common source) stage. By employing the MDS (Modified Derivative Super position) Technique, the LNA operate at different biasing conditions of transistors while maintaining the increased linearity due to compression of IM3 interferer. In order to estimate the advantage of this FC-LNA is implemented and simulated in 0.18 $\mu$ m CMOS process for 2.4 GHz using cadence virtuoso. From the measurement results The proposed LNA a Input Return Loss ( $S_{11}$ ) of -26.5 dB, Gain ( $S_{21}$ ) of 10.5 dB, Noise figure of 1.9 dB, and third order input intercept point (IIP3) of +2.96 dBm at supply voltage of 0.6V.

**KEYWORDS:** Folded cascode, MDS technique, Linearity, Noise figure.

## I. INTRODUCTION

Single chip RF receivers have been recently with CMOS technology for low cost terminals. The one of front end block of the receiver is LNA (Low Noise Amplifier). The main characteristics of LNA are Linearity, Noise Figure, sensitivity and Impedance matching. With the continuous shrinking of the feature size superior high frequencies characteristics of the devices have been demonstrated in CMOS technologies. It is difficult to accomplish a high gain and high linearity [1]. Over the LNA topologies, folded cascode LNA preferred for low voltage operations. In FC LNA, source of the nonlinearity is the transconductance nonlinearity of the CS (common source) stage. To overcome this limitation, some of the techniques have been reported in the part of the paper. In [2] the non-linearity can cancel by placing an auxiliary path. It eliminates the nonlinearity by adding the currents in the main and auxiliary paths at the output node. But the additional identical path increases the power dissipation in the LNA. To achieve high linearity, a more effective technique for narrowband applications reported in [3]. This technique gives high linearity by placing the harmonic termination network for blocking non-linear signals at a particular node.

The biasing condition of the transistors also effects on linearity of LNA. Optimum biasing of transistor is used to enhance linearity. The transistor is biased at zero crossing of the third order transconductance. By the source degeneration feedback, this technique reduces the third order intermodulation component (IM3).

$$i_{out} = g_{m1}V_i + g_{m2}V_i^2 + g_{m3}V_i^3 + \dots$$

In [5], the second-order-intermodulation component (IM2) generates externally and adding to increase the linearity at output. But, here the IM2 generator contributes the significant noise to the single ended LNA. The Derivative Superposition (DS) method is used to improve the linearity in the amplifier.

The DS [6] method is adding the non-linear components of two transistors by proper biasing of the transistors. And, due to the bias variations of the transistors the sensitivity reduced. Folded cascode LNA (FC-LNA) [8], feedback of IM2 component due to source degeneration inductance contributes to third-order-non-linearity. Gain enhancement technique is used to increase the gain. In [9], MDS (Modified Derivative Superposition) technique is proposed to increase linearity in FC-LNA. In FC-LNA at common source stage is replace the MDS technique, and thereby a high gain and linearity can be achieved for the LNA.

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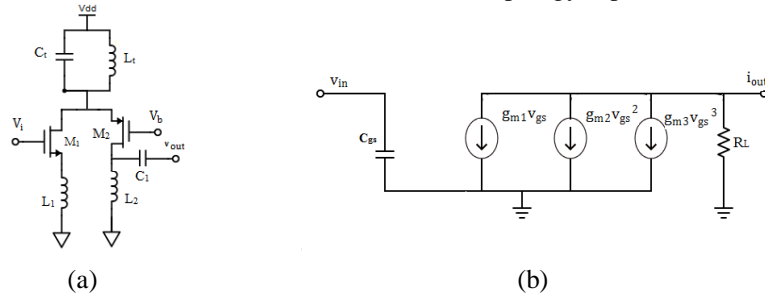
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## II. RELATED WORK

The cascode LNA topology is widely used LNA in receiver frontend. This single ended LNA is mainly used to achieve better gain, isolation, stability and impedance matching. The cascode LNA has source degeneration inductance to realize resistive impedance at input port without physical resistor. But due to stacking of the transistors, it has limitation in voltage margin. To overcome this drawback, folded cascode topology is preferred over cascode topology.



**Fig. 1 (a) Folded Cascode LNA (b) Small signal equivalent for a MOSFET**

As scales down the technology, the short channel effects are dominate and the drain current  $I_D$  of the transistor is represented by

$$I_D = \frac{1}{2} \frac{w}{L} \mu_0 C_{ox} \frac{(V_G - V_{TH})^2}{1 + \theta(V_G - V_{TH})} \quad (1)$$

Where  $\mu_0$  is low field mobility and  $\theta$  is fitting parameter. The drain current  $i_d$  of the MOS device is given by

$$i_{out} = g_{m1}V_i + g_{m2}V_i^2 + g_{m3}V_i^3 \quad (2)$$

In Fig.2 shows the small signal equivalent of MOSFET. In (5)  $g_{m1}$  is the main transconductance of MOSFET,  $g_{m2}$  is the second order non linear component and  $g_{m3}$  is the third order non linear component these coefficients are given by

$$g_{m1} = \frac{\partial i_d}{\partial V_{gs}}, g_{m2} = \frac{\partial^2 i_d}{\partial V_{gs}^2}, g_{m3} = \frac{\partial^3 i_d}{\partial V_{gs}^3} \quad (3)$$

## III. PROPOSED FC-LNA TOPOLOGY

As shown in the Fig.2, the proposed CMOS folded cascode LNA is designed for the characteristics of LNA over other LNA topologies. It had common source stage and common gate stage at input and output stages respectively. The two transistors  $M_1$  and  $M_2$  are part of the common source stage.  $M_3$  represent as the CG stage and this stage used for the isolation in the LNA. The LC tank circuit resonates at the required frequency. The LC tank circuit is realized using  $L_t$ ,  $C_t$  and interstage parasitic capacitances attained at the cascode stage. And it provides bias currents to the  $M_1$  and  $M_2$ . The  $g_m$ -bosting FC-LNA as shown in Fig.2. The non linearity of FC-LNA has mainly influenced by the CS stage at input stage. If we get better linearity at the input stage, that is highly influenced on linearity of LNA. At CS stage of this LNA is using the Modified Derivative Superposition method to get high Linearity. One of the main constraint of the Noise Figure (NF). The better gain in LNA eliminates the noise figure constraints in the front end wireless receiver.

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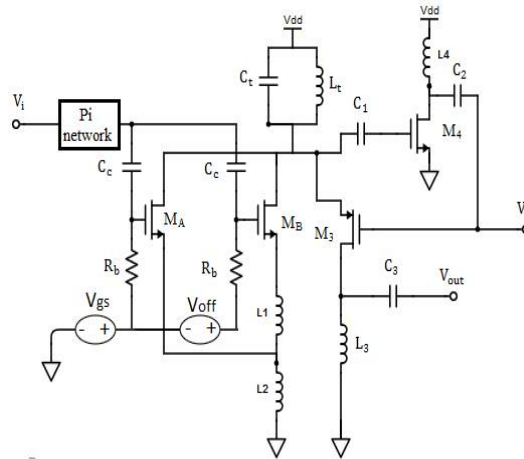


Fig. 2 Proposed Folded Cascode LNA

The efficient gain of the FC-LNA can be boosted by placing the inverting amplifier between gate and source of the CG stage [8] as shown in the Fig.2. By the small signal equivalent of the output stage of the FC-LNA makes the efficient transconductance of the CG stage  $(1+A)g_{m2}$  and the gain inverting amplifier which is connected between gate and source of CG stage.

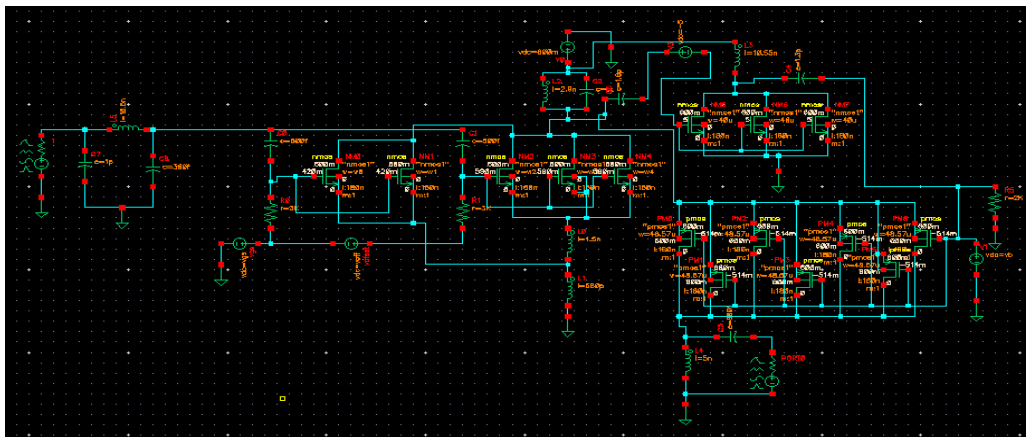


Fig. 3 Schematic Design for Proposed FC-LNA

The output voltage of the CG stage is given by

$$V_{out} = -(g_{m3}V_{gs3})R_L \quad (4)$$

Where A is gain of inverting amplifier,  $v_{gs3} = -(1 + A)V_{in}$ . From the inverting amplifier  $A = -g_{m4}(1 + \frac{C_2}{C_3})$ . Using (4), the voltage gain of the LNA is given by

$$A_v = \frac{V_{out}}{V_{in}} = g_{m3}R_L(1+A) \quad (5)$$

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**Impedance Matching:** There are different types of matching networks i.e. L, T, and Pi-network. In this LNA uses the Pi network for matching with transmission line i.e. 50Ω. The input impedance of the FC-LNA is  $R_{in} + jX_{in}$ . Pi-network gives the another facility of freedom for getting the input matching over the required Bandwidth.

$$Z_{in}(s) = s \left[ \left( \frac{C_{gs2}}{C_{gsT}} \right) L_1 + L_2 \right] + \frac{1}{sC_{gsT}} + \frac{g_{m11}L_2 + g_{m12}(L_1 + L_2)}{C_{gsT}} \quad (6)$$

## IV. MODIFIED DERIVATIVE SUPERPOSITION (MDS) TECHNIQUE

The source degenerated inductance  $L_s$  in folded cascode LNA in Fig.1 is placed to get real impedance at the input port. It had done the impedance matching at input. If we apply two fundamental frequencies  $\omega_1$  and  $\omega_2$  to the LNA, it makes the second order harmonics ( $\pm\omega_1, \pm\omega_2, \pm\omega_1 \pm \omega_2$ ) due to used the non linear devices in the amplifier to mix with fundamental frequencies. The third order harmonics are  $\pm 3\omega_1, \pm 3\omega_2, 2\omega_1 \pm \omega_2, 2\omega_2 \pm \omega_1$ . The two frequencies  $2\omega_1 \pm \omega_2, 2\omega_2 \pm \omega_1$  that are IM3 components leads to decrease the IIP3 of the amplifier. To improve IIP3 of cascode LNA, MGTR ( i.e. DS method) adopted in other amplifier. The DS (Derivative Superposition) improved the IIP3 by reducing the effect of higher order transconductance at CS stage in the LNA. But now the Modified Derivative Superposition Technique is used in this Cascode LNA to improve the IIP3 that is shown in Fig.3. The MDS method is proposed in the [5] to decrease the IM3.

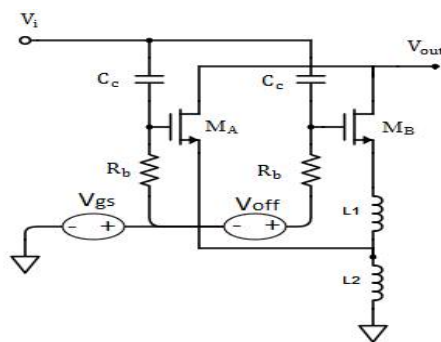


Fig. 4 MDS Technique

Fig.3 shows the realisation of MDS technique is at CS stage of the LNA. The MOS devices are in MDS technique  $M_A$  and  $M_B$ , and the inductor split into two inductors over the DS ethod in [5]. Actually DC chracteristics of the MOS device in three regions that are weak inversion(WI), moderate inversion(MI) and strong inversion(SI) regions

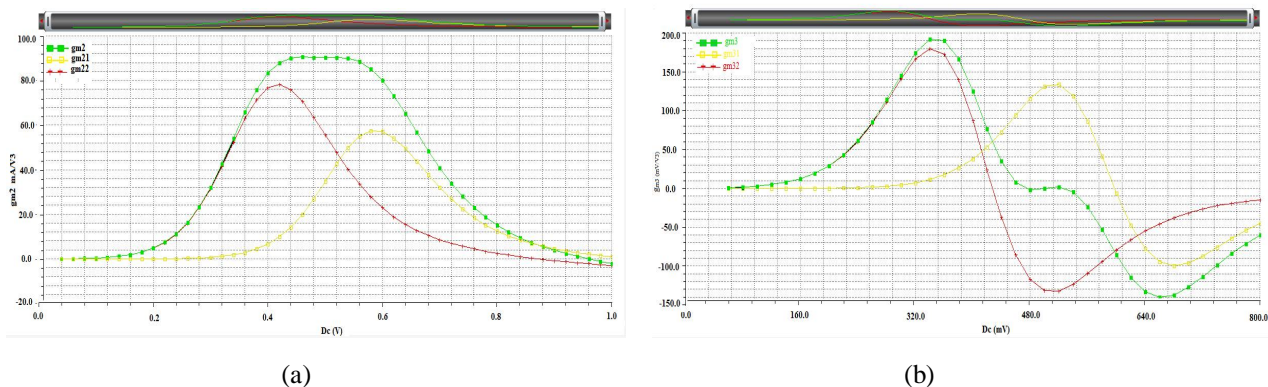


Fig. 5 (a) Overall gm2 (second order transconductance)(b) gm3 (third order transconductance) cancellation

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Most of LNAs used the SI region MOS device at CS stage because of the noise figure is reduced by that transistor. But for high linearity means to reduce IM3 components of MOS device it should be in the MI region. Hence  $M_A$  and  $M_B$  are biased in moderate and strong inversion regions respectively. In MDS technique, this method can cancel the second order non linearity to IM3 parameters by proper selection of  $L_1$  and  $L_2$ . The third order transconductance can cancel by proper selection width the transistors and biasing voltages to MOS devices. The  $g_{m3}$  (third order non linear component) and  $g_{m2}$  (second order non linear component) of MOS devices  $M_A$  and  $M_B$  are represented ( $g_{m2A}$  and  $g_{m2B}$ ) and ( $g_{m3A}$  and  $g_{m3B}$ ) respectively.

Proper selection of sizes and bias voltages to cancel negative peak of  $g_{m3B}$  by positive peak of  $g_{m3A}$ .  $L_1$  source degenerated inductance gives phase to the  $g_{m3A}$  and the resultant magnitude of  $g_{m3A}$  and  $g_{m3B}$  is  $g_{m3}$ . And that resultant should out of phase with the  $g_{m2}$  ( $= g_{m2A} + g_{m2B}$ ). Thus by the source degeneration inductor  $L_1$  the contribution of  $g_{m2}$  to non linearity reduced by adjusting of the phase of the  $g_{m3}$ . At a particular bias voltages of  $M_1$  and  $M_2$  have the highest  $g_{m2}$  and  $g_{m3}$  are shown in Fig.5(a)-(b).

## V. LINEARITY ANALYSIS OF FC-LNA

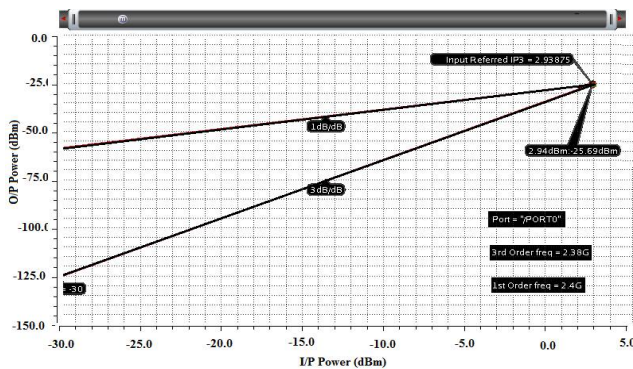
The common source (CS) stage in proposed FC-LNA used the MDS technique to enhance the linearity. The total output current from the two transistors i.e.  $i_{out}$  is represented as

$$i_{out}(v_i) = L_1(S_1)v_i + L_2(S_1, S_2)v_i^2 + L_3(S_1, S_2, S_3)v_i^3 \quad (7)$$

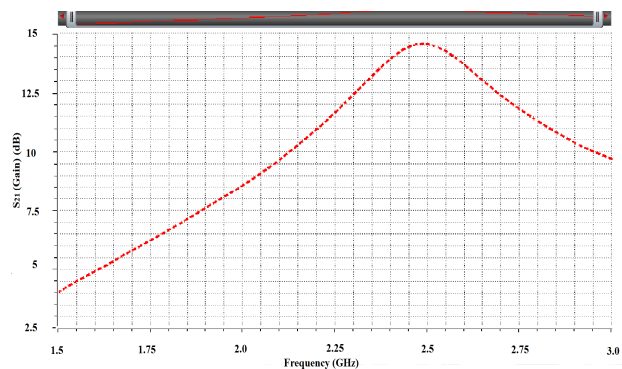
Where  $v_i$  is the input voltage and  $L_n(S_1, S_2, S_3 \dots S_n)$  is the  $n^{th}$  order nonlinear transfer function. The nonlinear and dynamic systems are used the volterra series for finding the coefficients of the equation.

Normally in the wireless communication systems used the multi frequency message signal. Here the LNA using the two closely spaced frequencies that are  $\omega_1$  and  $\omega_2$ . And the voltage equation represented by

$$v_{out} = A[\cos(\omega_1 t) + \cos(\omega_2 t)] \quad (8)$$



(a)



(b)

The total current represented as

$$i_{out} = g_{m3A}v_1^3 + g_{m1B}v_2 + g_{m2B}v_2^2 + g_{m3B}v_2^3 \quad (9)$$

Because of the  $M_A$  is in MI region, the second and third order transconductance of the transistor are neglected. Generally, the IIP3 of the LNA is represented as

$$IIP_3(2\omega_2 - \omega_1) = \frac{1}{6Re(Z_{in}(S))} \left| \frac{L_1(S_1)}{L_3(S_1, S_2, S_3)} \right| \quad (10)$$

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The coefficients are solved by volterra series and the IIP3 simplified & represented as

$$IIP_3(2\omega_2 - \omega_1) = \frac{1}{6\text{Re}(Z_{in}(s))} \left| \frac{4g_{m1B}^2 \omega^2 [L_2 C_{gsT} + L_1 C_{gsB}]}{|\epsilon|} \right| \quad (11)$$

Where  $Z_{in}(S)$  is the input impedance, and

$$\epsilon = g_{m3A}(1 + j\omega L_1 g_{m1B}) [1 + (\omega L_1 g_{m1B})^2] \left[ 1 + \frac{L_1 C_{gsB}}{L_2 C_{gsT} + L_1 C_{gsB}} \right] + g_{m3B} - \frac{2g_{m2B}^2}{3g_{m1B}} \left( \frac{j2\omega g_{m1B} [L_1 + L_2]}{1 + j2\omega g_{m1B} [L_1 + L_2]} \right) \quad (12)$$

For  $g_{m3}$  cancellation, the  $g_{m3B}$  and  $g_{m3A}$  are of opposite to each other. So in the above equation 1<sup>st</sup> and 2<sup>nd</sup> terms are cancelled by selecting proper values of  $L_1$  and  $L_2$ . The  $\epsilon$  equation had the real and imaginary parts. If  $\epsilon=0$ , then IIP3 value is infinite. So in order to IMD3 to be zero, both real and imaginary parts of  $\epsilon$  must be zero for proper selection of  $L_1$  and  $L_2$  from eq. (10). The fundamental tone  $\omega_1$  and IM3 interferer ( $2\omega_2 - \omega_1$ ) are highly effects on the power gain, so this LNA concentrated on these frequencies to get high linearity and gain.

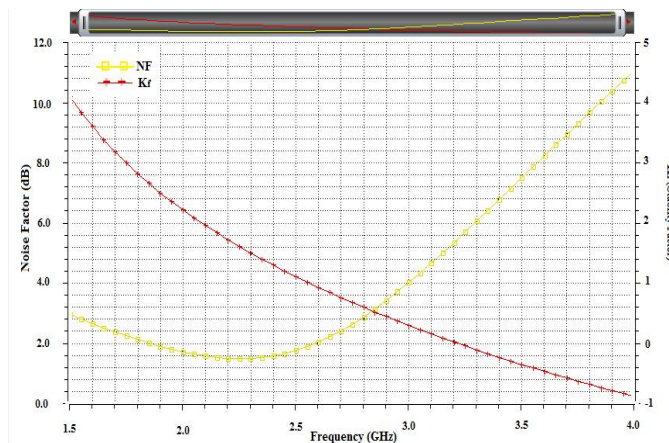


Fig. 7 Noise Figure & Stability Factor

The Noise Figure of the Receiver mainly depends on the foremost blocks. Hence the LNA is taken the care about NF.

## VI. SIMULATION RESULTS

The proposed FC-LNA is simulated in 0.18 $\mu$ m CMOS process by cadence virtuoso environment. The FC-LNA topology operated for 2.4 GHz at supply voltage of 0.6V. The scattering parameters  $S_{11}$  and  $S_{21}$  are important for the every LNA.

The third order intermodulation (IMD3) components are determining by applying two tones 2.4 GHz and 2.42 GHz as input. The MDS technique is remove IM3 interferer at the 2.38 GHz frequency. And this interferer is dominating source of the nonlinearity.

The measurement results are gain ( $S_{21}$ ), Input Return Loss ( $S_{11}$ ), Noise figure, IIP3, and stability factor ( $K_f$ ) of proposed FC-LNA shown in Fig.7-9. The input return loss is -11dB, Noise Figure of 1.8 dB. The FC-LNA shows the better stability over desired frequency. The stability Factor ( $K_f$ ) is represented as

$$K_f = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \quad \text{where } \Delta = S_{11}S_{22} - S_{21}S_{12} \quad (13)$$

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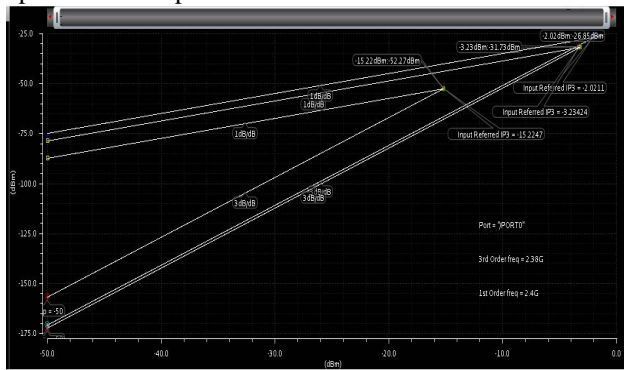
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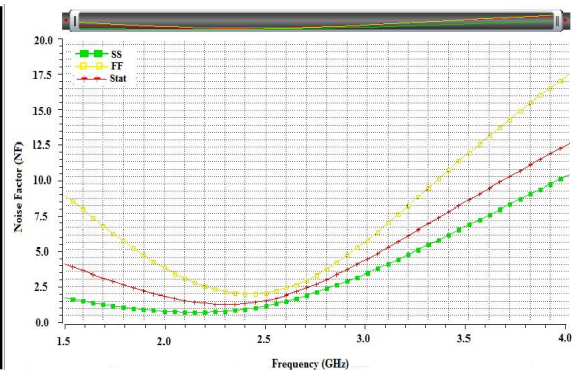
**Table 1 Component Values**

Component	M <sub>1</sub>	M <sub>2</sub>	M <sub>3</sub>	M <sub>4</sub>	L <sub>1</sub>	L <sub>2</sub>	L <sub>3</sub>	L <sub>4</sub>	L <sub>1</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	R <sub>b</sub>
Values	39 μm	81 μm	340 μm	120 μm	1.5 nH	0.58 nH	5 nH	10.8 nH	2.9 nH	0.8 pF	1.6 pF	1.3 pF	0.5 pF	3 KΩ

Table.1 has component values of the proposed FC-LNA. The bias voltages of the M<sub>A</sub> and M<sub>B</sub> are 0.47V and 0.51V respectively. Table.2. shows the performance of the proposed FC-LNA over other LNAs from the literature papers [7, 8, 14, 16, 19-21]. From [19], emphasize is given for reducing the NF and decreasing the non linearity with trade-off with power consumption.



(a)



(b)

The proposed FC-LNA determines the performance in the various corners of gain (S<sub>21</sub>), input return loss (S<sub>11</sub>) and IIP3 are given in Figures.6-9.

**Table 2 Comparison Values**

	This work	[18]	[19]	[16]	[14]
<b>Process (μm)</b>	0.18	0.18	0.18	0.18	0.18
<b>Frequency(GHz)</b>	2.4	5	5	2.4	5
<b>Supply Voltage</b>	0.6	0.6	0.6	1.8	1.2
<b>Gain S21 (dB)</b>	10.5	9.2	10.2	11.2	15
<b>Input Return Loss S11 (dB)</b>	-26.5	-12	-17.9	-11	-10
<b>Noise Figure(dB)</b>	1.9	4.5	4.1	2.15	2
<b>IIP3 (dBm)</b>	2.94	-16	-15	-6.15	-2

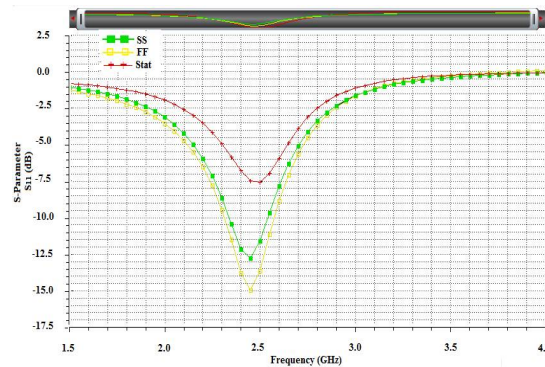
Those are SS (slow-slow), FF (fast-fast) corners over the proposed FC-LNA. The variations of drain current in SS and FF are due to different thickness of gate oxide, mobility, threshold voltage.

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**Fig. 9 Input Return Loss (S11) at various corners**

The passive components of MOS devices in the SS corner are MAX, so it's slower in speed. But the FF corner of transistor, MIN corner of passive components.

## VII. CONCLUSION

A Narrow Band (NB) FC-LNA with MDS technique was proposed in this paper. And its relevant parameters are analyzed. The dominated source of nonlinearity in FC-LNA is CS stage is replaced by the Modified Derivative Superposition (MDS) Technique. This method boosted the IIP3 for the Folded Cascode LNA. It gives the better noise figure and high gain at required frequency range. This is used at foremost block at receiver end where the requirement of high linearity and better noise figure (NF) such as Wi-Fi receiver.

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